Texas Instruments
TPS259250, TPS259251, TPS259260, TPS259261
SLVSCQ3 – AUGUST 2015

TPS25925x/6x Simple 5-V/12-V eFuse Protection Switches

1 Features

- 12-V eFuse – TPS25926x
- 5-V eFuse – TPS25925x
- Integrated 30-mΩ Pass MOSFET
- Fixed Over-Voltage Clamp:
  - 6.1-V Clamp - TPS25925x
  - 15-V Clamp - TPS25926x
- 2-A to 5-A Adjustable I_{LIMIT} (±15% Accuracy)
- Programmable V_{OUT} Slew Rate, UVLO
- Built-in Thermal Shutdown
- UL 2367 Recognition Pending
- Safe During Single Point Failure Test (UL60950)
- Small Foot Print – 10L (3mm x 3mm) VSON

2 Applications

- HDD and SSD Drives
- Set Top Boxes
- Servers / AUX Supplies
- PCI/PCIe Cards
- Adapter Powered Devices

3 Description

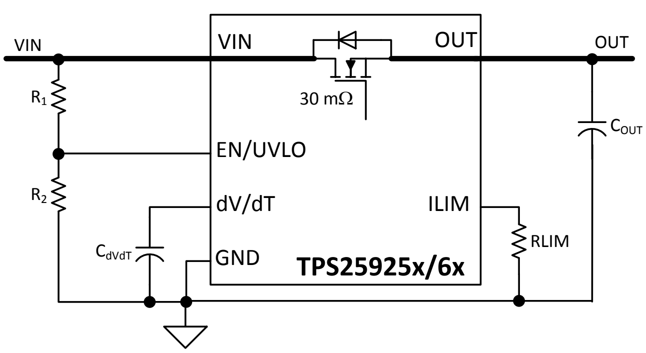
The TPS25925x/6x family of eFuses is a highly integrated circuit protection and power management solution in a tiny package. The devices use few external components and provide multiple protection modes. They are a robust defense against overloads, shorts circuits, voltage surges, excessive inrush current, and reverse current. Current limit level can be set with a single external resistor and current limit set has a typical accuracy of ±15%. Over voltage events are limited by internal clamping circuits to a safe fixed maximum, with no external components required. TPS25926x devices provide over voltage protection (OVP) for 12-V systems and TPS25925x devices for 5-V systems. In cases with particular voltage ramp requirements, a dV/dT pin is provided that can be programmed with a single capacitor to ensure proper output ramp rates.

Device Information(1)

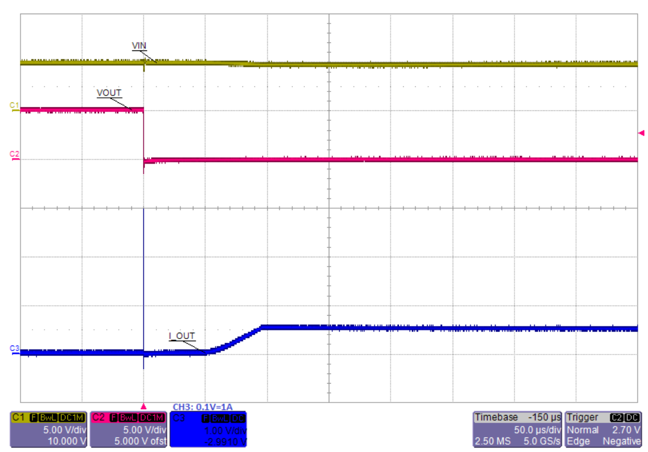
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS259250, TPS259251	VSON (10)	3.00 mm × 3.00 mm
TPS259260, TPS259261		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Schematic



Transient: Output Short Circuit



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4 Revision History

DATE	REVISION	NOTES
August 2015	*	Initial release.

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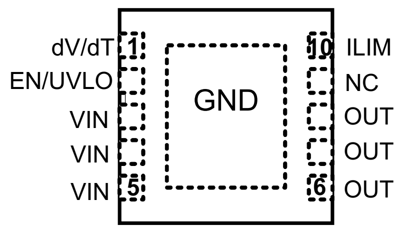
5 Device Comparison Table

PART NUMBER	UV	OV CLAMP	FAULT RESPONSE	STATUS
TPS259250	4.3 V	6.1 V	Latched	Active
TPS259251	4.3 V	6.1 V	Auto Retry	Active
TPS259260	4.3 V	15 V	Latched	Active
TPS259261	4.3 V	15 V	Auto Retry	Active

6 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
dV/dT	1	Connect a capacitor from this pin to GND to control the ramp rate of OUT voltage at device turn-on.
EN/UVLO	2	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET. When pulled high, it enables the device. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider.
GND	Thermal Pad	GND
ILIM	10	A resistor from this pin to GND will set the overload and short circuit limit.
NC	9	Not Connected Internally. Can be left floating or grounded.
OUT	6-8	Output of the device
VIN	3-5	Input supply voltage

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7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Supply voltage (1)	VIN	–0.3	20	V
	VIN (Transient < 1 ms)		22	
Output voltage	OUT	–0.3	VIN + 0.3	V
	OUT (Transient < 1 µs)		-1.2	V
Voltage	ILIM	–0.3	7	V
Continuous output current			6.25 (3)	A
Voltage	EN/UVLO	–0.3	7	V
Voltage	dV/dT	–0.3	7	V
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Device supports high peak current during short circuit conditions until current is internally limited.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Input voltage	VIN (TPS25926x)	4.5	12	13.8	V
	VIN (TPS25925x)	4.5	5	5.5	
	dV/dT, EN/UVLO	0		6	
	ILIM	0		3	
Continuous output current	I_{OUT}	0		5	A
Resistance	ILIM	10	100	162	kΩ
External capacitance	OUT	0.1	1	1000	µF
	dV/dT		1	1000	nF
Operating junction temperature range, T_J		–40	25	125	°C
Operating Ambient temperature range, T_A		–40	25	85	°C

7.4 Thermal Information(1)

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC		TPS25925x/6x DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	53	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.2	
ψ_{JT}	Junction-to-top characterization parameter	1.2	
ψ_{JB}	Junction-to-board characterization parameter	21.4	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	5.9	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

–40°C ≤ T_J ≤ 125°C, VIN = 12 V for TPS25926x, VIN = 5 V for TPS25925x, $V_{EN\ /UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{dVdT} = OPEN. All voltages referenced to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN (INPUT SUPPLY)						
V_{UVR}	UVLO threshold, rising		4.15	4.3	4.45	V
V_{UVhyst}	UVLO hysteresis(1)			5%		
IQ_{ON}	Supply current	Enabled: EN/UVLO = 2 V, TPS25926x	0.2	0.47	0.65	mA
		Enabled: EN/UVLO = 2 V, TPS25925x	0.4	0.42	0.85	mA
IQ_{OFF}		EN/UVLO = 0 V		0.13	0.25	mA
V_{OVC}	Over-voltage clamp	VIN > 16.5 V, I_{OUT} = 10 mA, TPS25926x	13.8	15	16.5	V
		TPS25925x, VIN > 6.75 V, I_{OUT} = 10 mA, –40℃ ≤ T_J ≤ 85℃	5.5	6.1	6.75	
		TPS25925x, VIN > 6.75 V, I_{OUT} = 10 mA, –40℃ ≤ T_J ≤ 125℃	5.25	6.1	6.75	
EN/UVLO (ENABLE/UVLO INPUT)						
V_{ENR}	EN Threshold voltage, rising		1.37	1.4	1.44	V
V_{ENF}	EN Threshold voltage, falling		1.32	1.35	1.39	V
I_{EN}	EN Input leakage current	0 V ≤ V_{EN} ≤ 5 V	–100	0	100	nA
dV/dT (OUTPUT RAMP CONTROL)						
I_{dVdT}	dV/dT Charging current(1)	V_{dVdT} = 0 V		220		nA
R_{dVdT_disch}	dV/dT Discharging resistance	EN/UVLO = 0 V, I_{dVdT} = 10 mA sinking	50	73	100	Ω
$V_{dVdTmax}$	dV/dT Max capacitor voltage(1)			5.5		V
$GAIN_{dVdT}$	dV/dT to OUT gain(1)	ΔV_{dVdT}		4.85		V/V
ILIM (CURRENT LIMIT PROGRAMMING)						
I_{ILIM}	ILIM Bias current(1)			10		µA
I_{OL}	Overload current limit(2)	R_{ILIM} = 45.3 kΩ, $V_{VIN-OUT}$ = 1 V	1.75	2.1	2.45	A
		R_{ILIM} = 100 kΩ, $V_{VIN-OUT}$ = 1 V	3.4	3.75	4.05	
		R_{ILIM} = 150 kΩ, $V_{VIN-OUT}$ = 1 V	4.5	5.1	5.7	
$I_{OL-R-Short}$		R_{ILIM} = 0 Ω, Shorted Resistor Current Limit (Single Point Failure Test: UL60950)(1)		0.84		A
$I_{OL-R-Open}$		R_{ILIM} = OPEN, Open Resistor Current Limit (Single Point Failure Test: UL60950)(1)		0.73		A

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(2) Pulsed testing techniques used during this test maintain junction temperature approximately equal to ambient temperature.

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Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, VIN = 12 V for TPS25926x, VIN = 5 V for TPS25925x, $V_{EN\ /UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{dVdT} = OPEN. All voltages referenced to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SCL}	Short-circuit current limit(2)	R_{ILIM} = 45.3 kΩ, $V_{VIN-OUT}$ = 5 V, TPS25925x	1.7	2.05	2.4	A
		R_{ILIM} = 45.3 kΩ, $V_{VIN-OUT}$ = 12 V, TPS25926x	1.62	1.98	2.35	
		R_{ILIM} = 100 kΩ, $V_{VIN-OUT}$ = 5 V, TPS25925x	3.1	3.56	4.0	
		R_{ILIM} = 100 kΩ, $V_{VIN-OUT}$ = 12 V, TPS25926x	2.9	3.32	3.85	
		R_{ILIM} = 150 kΩ, $V_{VIN-OUT}$ = 5 V, TPS25925x	4.12	4.86	5.58	
		R_{ILIM} = 150 kΩ, $V_{VIN-OUT}$ = 12 V, TPS25926x	3.7	4.5	5.5	
$RATIO_{FASTRIP}$	Fast-Trip comparator level w.r.t. overload current limit(1)	$I_{FASTRIP}$: I_{OL}		160%		
$V_{OpenILIM}$	ILIM Open resistor detect threshold(1)	V_{ILIM} Rising, R_{ILIM} = OPEN		3.1		V
OUT (PASS FET OUTPUT)						
T_{ON}	Turn-on delay(1)	EN/UVLO → H to I_{VIN} = 100 mA, 1-A resistive load at OUT		220		µs
$R_{DS(on)}$	FET ON resistance	T_J = 25°C	21	30	39	mΩ
		T_J = 125°C		40	50	
$I_{OUT-OFF-LKG}$	OUT Bias current in off state	$V_{EN/UVLO}$ = 0 V, V_{OUT} = 0 V (Sourcing)	–5	0	1.2	µA
$I_{OUT-OFF-SINK}$		$V_{EN/UVLO}$ = 0V, V_{OUT} = 300 mV (Sinking)	10	15	20	
THERMAL SHUT DOWN (TSD)						
T_{SHDN}	TSD Threshold, rising(1)			150		°C
$T_{SHDNhyst}$	TSD Hysteresis(1)			10		°C
	Thermal fault: latched or autoretry	TPS259250, TPS259260		LATCHED		
		TPS259251, TPS259261		AUTO-RETRY		

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFFdly}	Turn Off delay(1)	EN↓		0.4		µs
dV/dT (OUTPUT RAMP CONTROL)						
t_{dVdT}	Output ramp time	TPS25926x, EN/UVLO → H to OUT = 11.7 V, C_{dVdT} = 0	0.7	1	1.3	ms
		TPS25925x, EN/UVLO → H to OUT = 4.9 V, C_{dVdT} = 0	0.28	0.4	0.52	
		TPS25926x, EN/UVLO → H to OUT = 11.7 V, C_{dVdT} = 1 nF(1)		12		
		TPS25925x, EN/UVLO → H to OUT = 4.9 V, C_{dVdT} = 1 nF(1)		5		
ILIM (CURRENT LIMIT PROGRAMMING)						
$t_{FastOffDly}$	Fast-Trip comparator delay(1)	I_{OUT} > $I_{FASTRIP}$ to I_{OUT}= 0 (Switch Off)		300		ns
THERMAL SHUTDOWN (TSD)						
t_{TSDdly}	Retry Delay after TSD Recovery, T_J < [T_{SHDN} - 10°C](1)	At VIN = 5 V, TPS259251 and TPS259261		110		ms
		At VIN = 12 V, TPS259251 and TPS259261		145		

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.7 Typical Characteristics

T_J = 25°C, V_{VIN} = 12 V for TPS25926x, V_{VIN} = 5 V for TPS25925x, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1µF, C_{dVdT} = OPEN (unless stated otherwise)

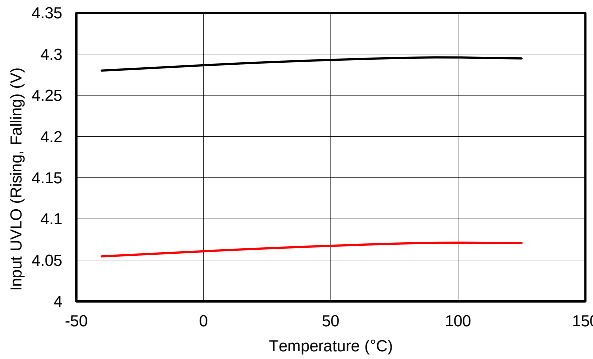


Figure 1. Input UVLO vs Temperature

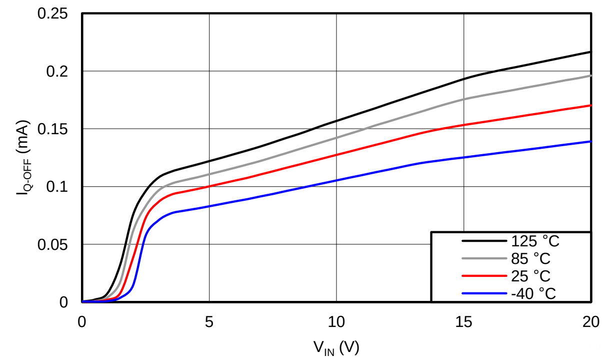
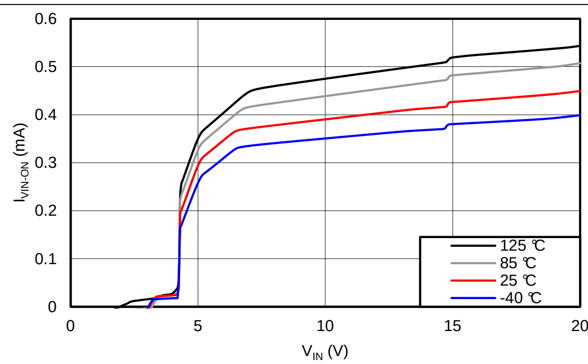
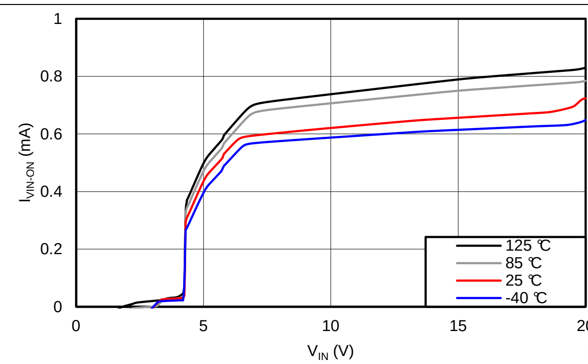


Figure 2. IQ_{OFF} vs V_{IN}



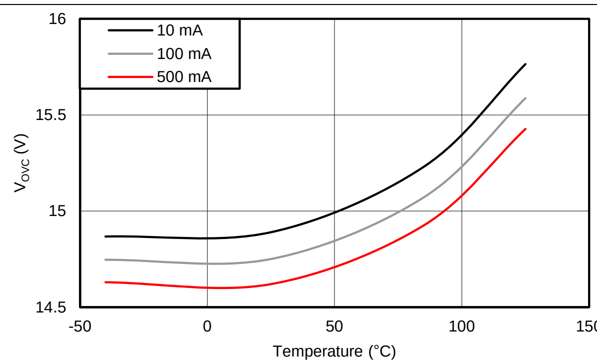
TPS25926x

Figure 3. I_{VIN-ON} vs V_{IN}



TPS25925x

Figure 4. I_{VIN-ON} vs V_{IN}



TPS25926x

Figure 5. V_{OVC} vs Temperature Across I_{OUT}

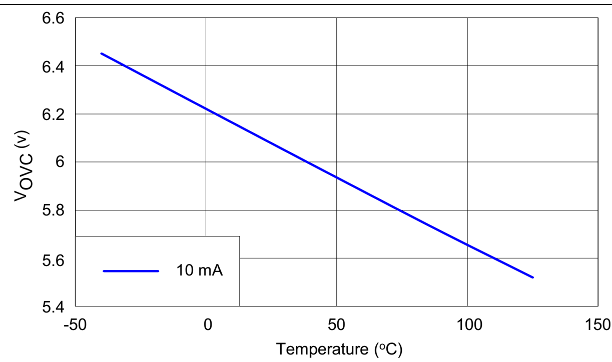


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Figure 6. V_{OVC} vs Temperature

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Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V for TPS25926x, V_{VIN} = 5 V for TPS25925x, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1µF, C_{dVdT} = OPEN (unless stated otherwise)

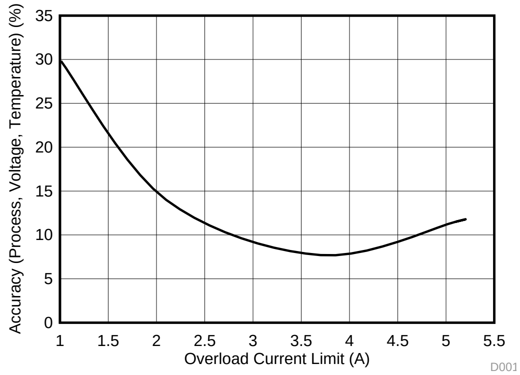


Figure 7. Accuracy vs Overload Current Limit

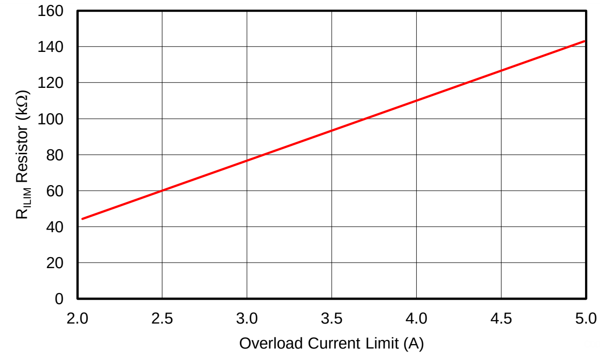
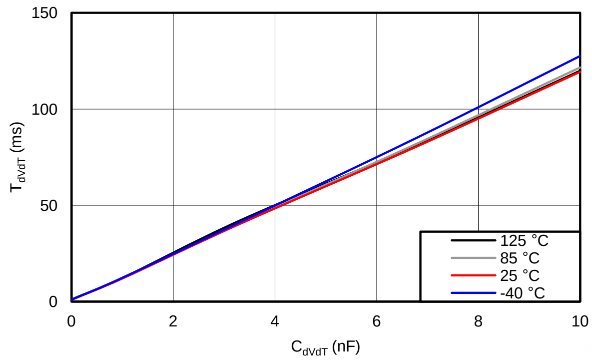
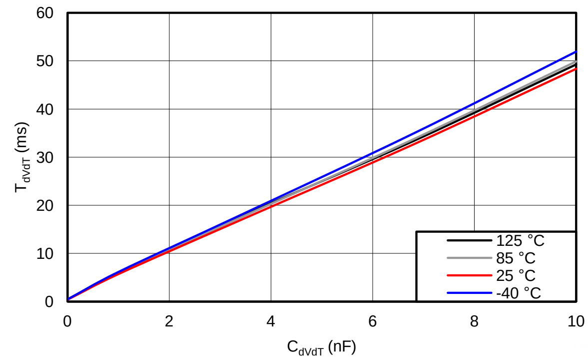


Figure 8. I_{RILM} Resistor vs Overload Current Limit



TPS25926x

Figure 9. T_{dVdT} vs C_{dVdT}



TPS25925x

Figure 10. T_{dVdT} vs C_{dVdT}

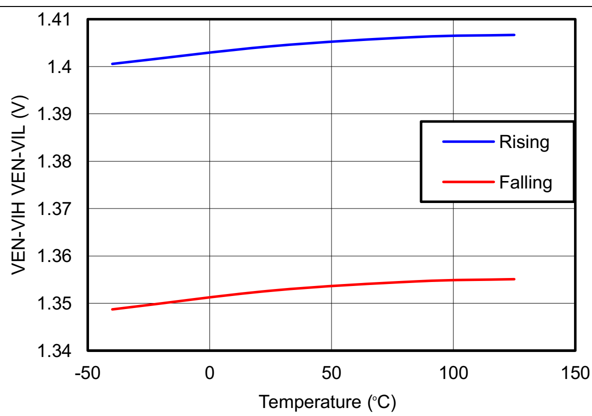


Figure 11. V_{EN_VIH}, V_{EN_VIL} vs Temperature

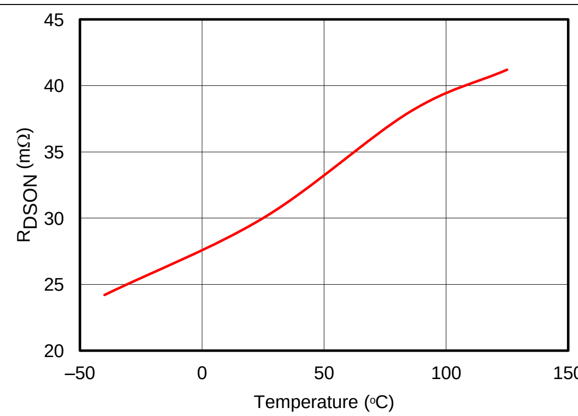


Figure 12. R_{DSON} vs Temperature

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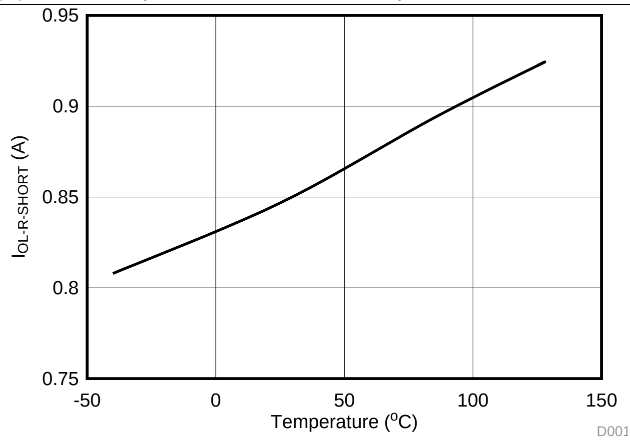
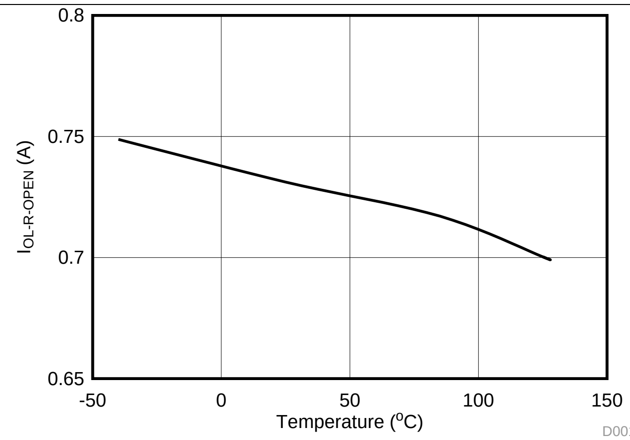
Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V for TPS25926x, V_{VIN} = 5 V for TPS25925x, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1µF, C_{dVdT} = OPEN (unless stated otherwise)



R_{ILIM} = 0Ω

Figure 13. $I_{OL-R-Short}$ vs Temperature



R_{ILIM} = OPEN

Figure 14. $I_{OL-R-Open}$ vs Temperature

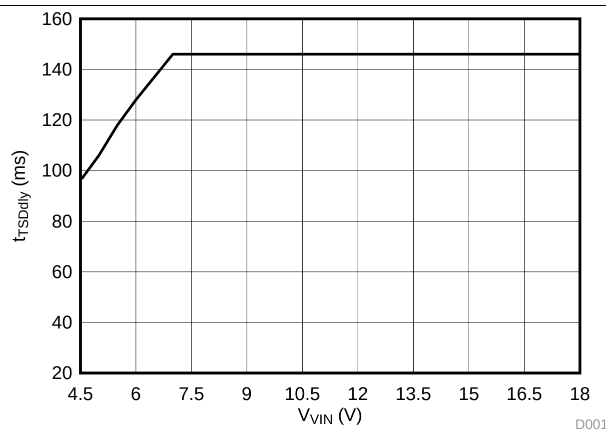
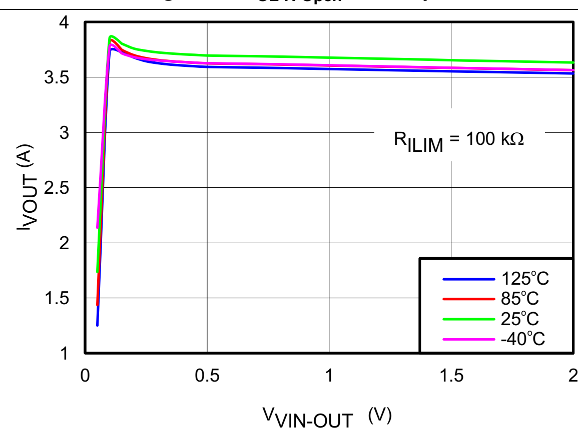
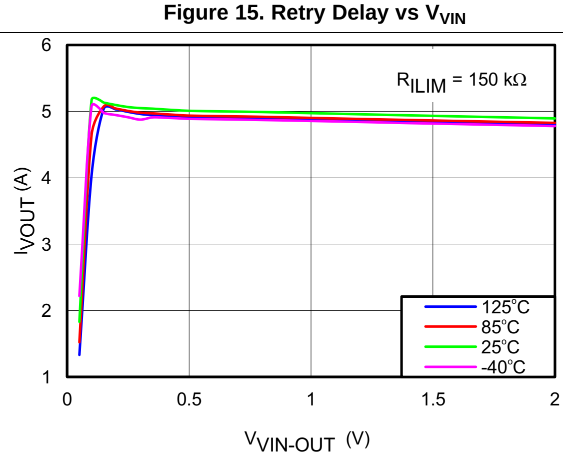


Figure 15. Retry Delay vs V_{VIN}



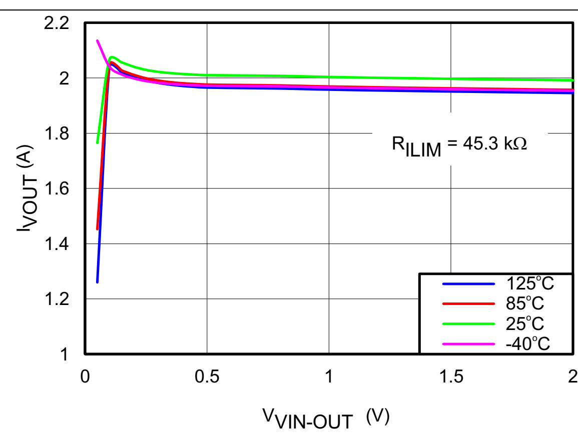
R_{ILIM} = 100 kΩ

Figure 16. I_{OUT} vs $V_{VIN-OUT}$



R_{ILIM} = 150 kΩ

Figure 17. I_{OUT} vs $V_{VIN-OUT}$



R_{ILIM} = 45.3 kΩ

Figure 18. I_{OUT} vs $V_{VIN-OUT}$

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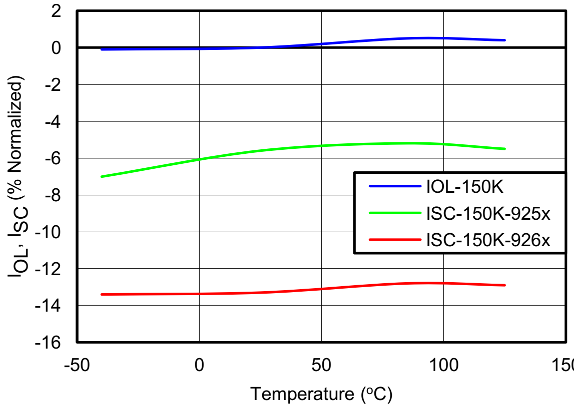
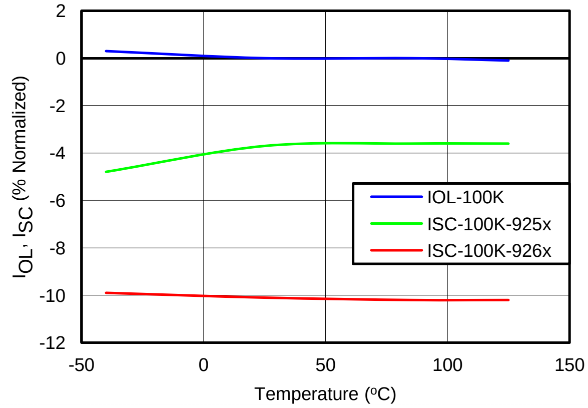
Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V for TPS25926x, V_{VIN} = 5 V for TPS25925x, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1µF, C_{dVdT} = OPEN (unless stated otherwise)



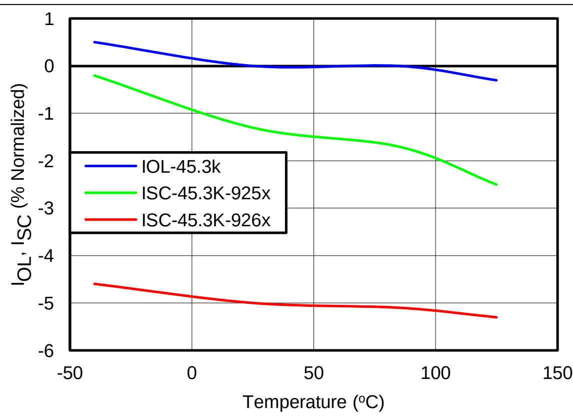
R_{ILIM} = 150 kΩ

Figure 19. I_{OL}, I_{SC} vs Temperature



R_{ILIM} = 100 kΩ

Figure 20. I_{OL}, I_{SC} vs Temperature



R_{ILIM} = 45.3 kΩ

Figure 21. I_{OL}, I_{SC} vs Temperature

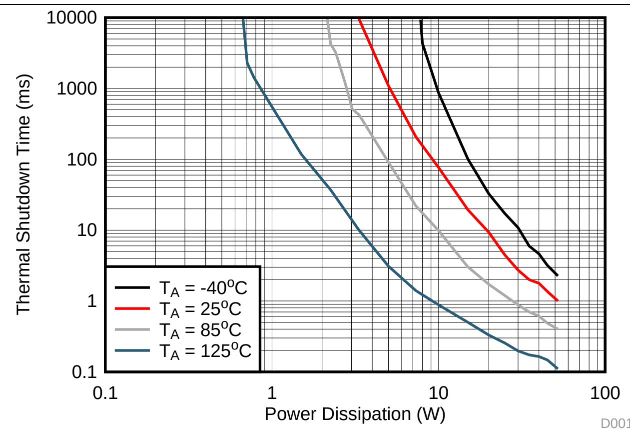
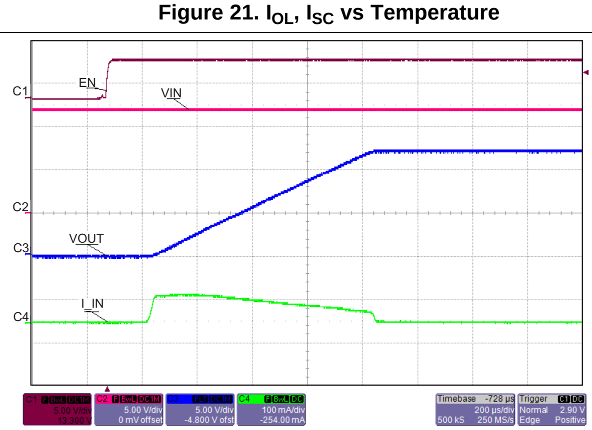
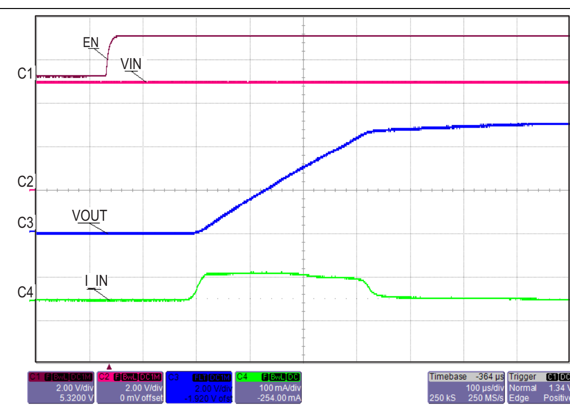


Figure 22. Thermal Shutdown Time vs Power Dissipation



TPS25926x, C_{dVdT} = OPEN, C_{OUT} = 4.7 µF

Figure 23. Transient: Output Ramp

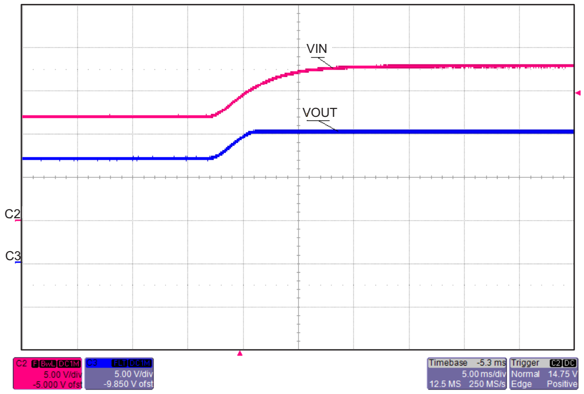


TPS25925x, C_{dVdT} = OPEN, C_{OUT}= 4.7 µF

Figure 24. Transient: Output Ramp

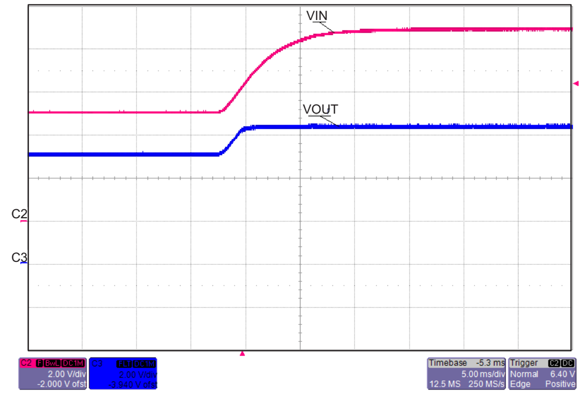
Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V for TPS25926x, V_{VIN} = 5 V for TPS25925x, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1µF, C_{dVdT} = OPEN (unless stated otherwise)



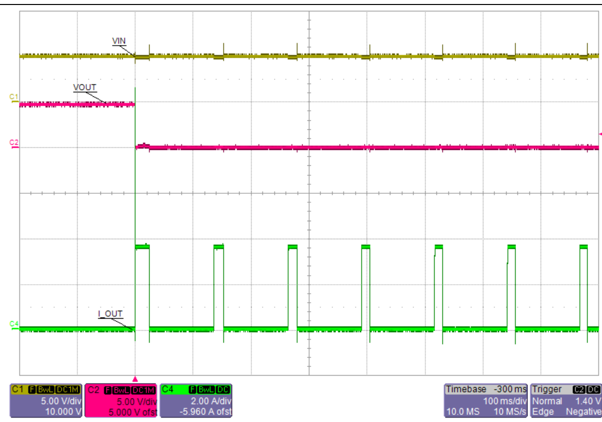
TPS25926x

Figure 25. Transient: Over-Voltage Clamp



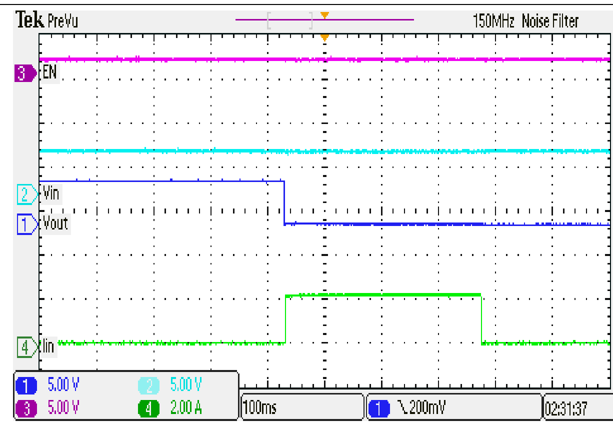
TPS25925x

Figure 26. Transient: Over-Voltage Clamp



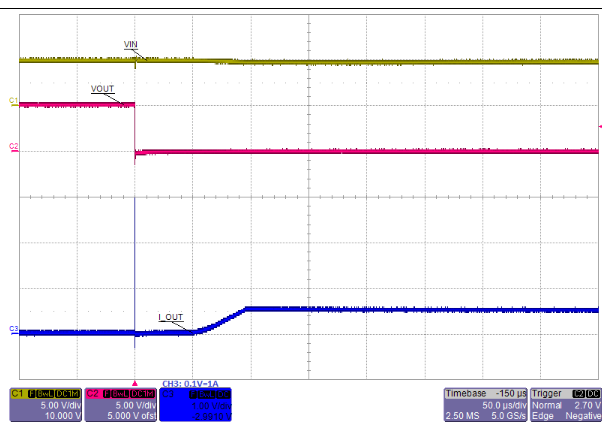
TPS259251/61, V_{VIN} = 5 V

Figure 27. Transient: Thermal Fault Auto-Retry



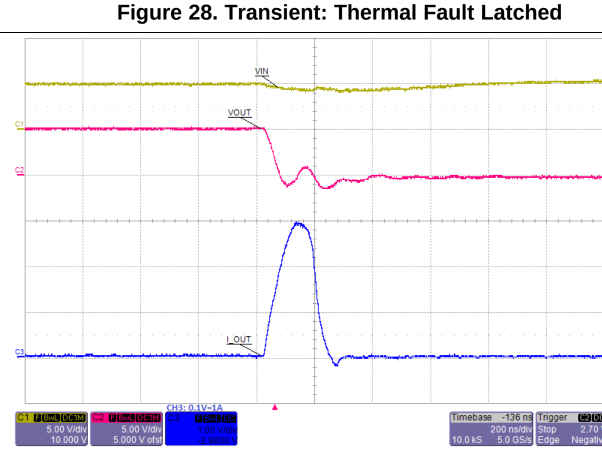
TPS259250/60 , V_{VIN} = 5 V

Figure 28. Transient: Thermal Fault Latched



TPS25925x/6x, V_{VIN} = 5 V, R_{ILIM} = 150 kΩ

Figure 29. Transient: Output Short Circuit



TPS25925x/6x, V_{VIN} = 5 V, R_{ILIM} = 150 kΩ

Figure 30. Short Circuit (Zoom): Fast-Trip Comparator

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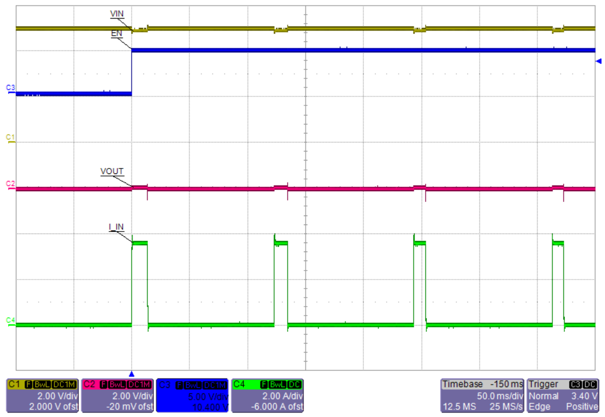
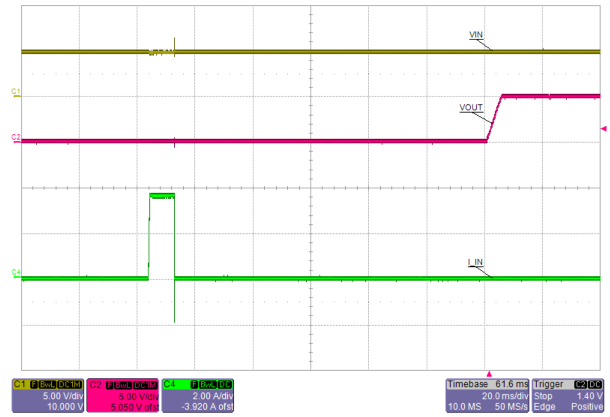
Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V for TPS25926x, V_{VIN} = 5 V for TPS25925x, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1µF, C_{dVdT} = OPEN (unless stated otherwise)



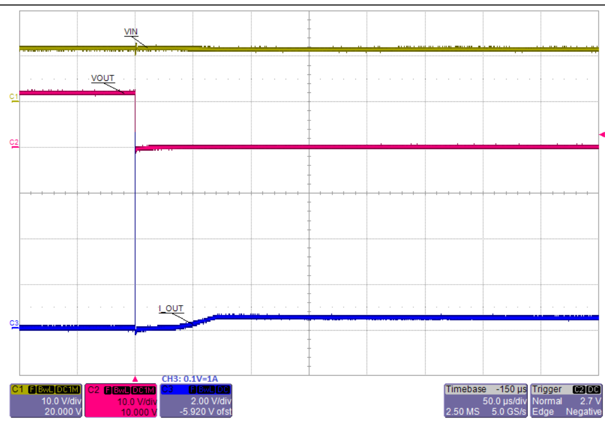
TPS259251/61 , V_{VIN} = 5 V

Figure 31. Transient: Wake Up to Short Circuit



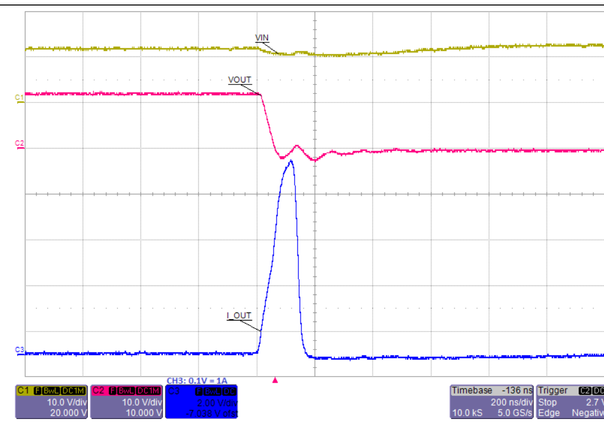
TPS259251/61 , V_{VIN} = 5 V, C_{dVdT} = 1nF

Figure 32. Transient: Recovery from Short Circuit



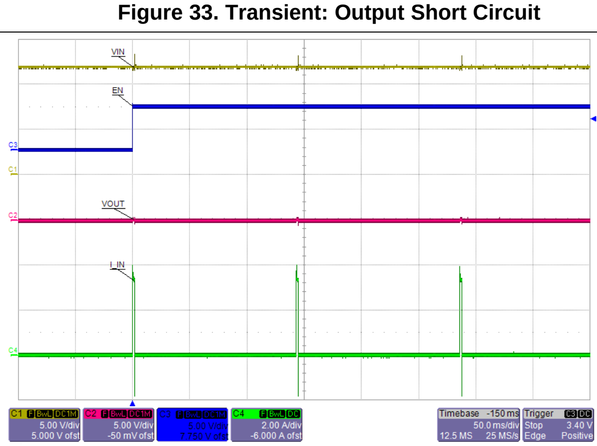
TPS25926x , V_{VIN} = 12 V, R_{ILIM} = 150 kΩ

Figure 33. Transient: Output Short Circuit



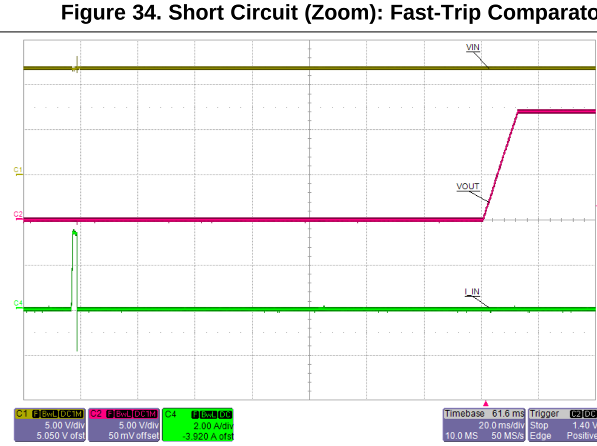
TPS25926x, V_{VIN} = 12 V, R_{ILIM} = 150 kΩ

Figure 34. Short Circuit (Zoom): Fast-Trip Comparator



TPS25926x, V_{VIN} = 12 V

Figure 35. Transient: Wake Up to Short Circuit

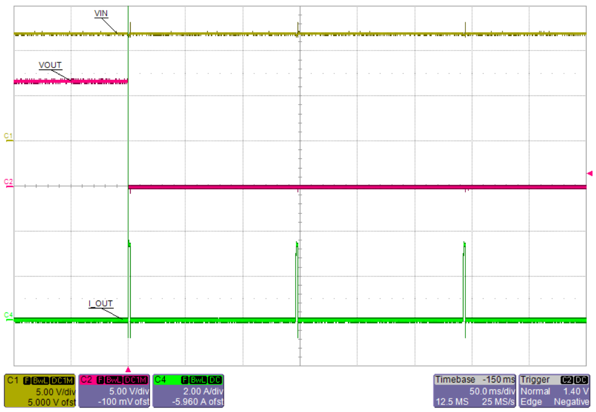


TPS25926x, V_{VIN} = 12 V, C_{dVdT} = 1 nF

Figure 36. Transient: Recovery from Short Circuit

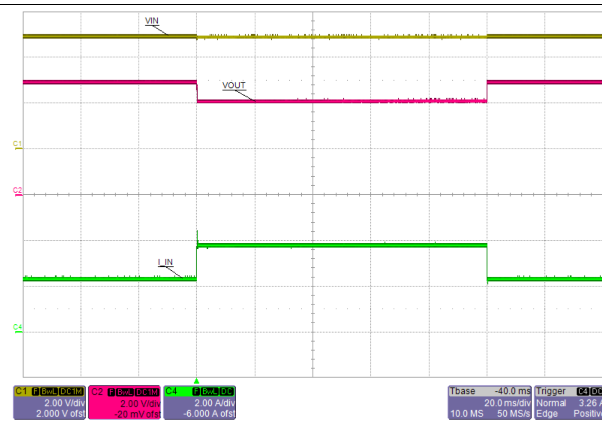
Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V for TPS25926x, V_{VIN} = 5 V for TPS25925x, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1µF, C_{dVdT} = OPEN (unless stated otherwise)



TPS25926x, V_{VIN} = 12 V

Figure 37. Transient: Thermal Fault Auto-Retry



I_{LOAD} stepped From 65% to 125%, back to 65%

Figure 38. Transient: Overload Current Limit

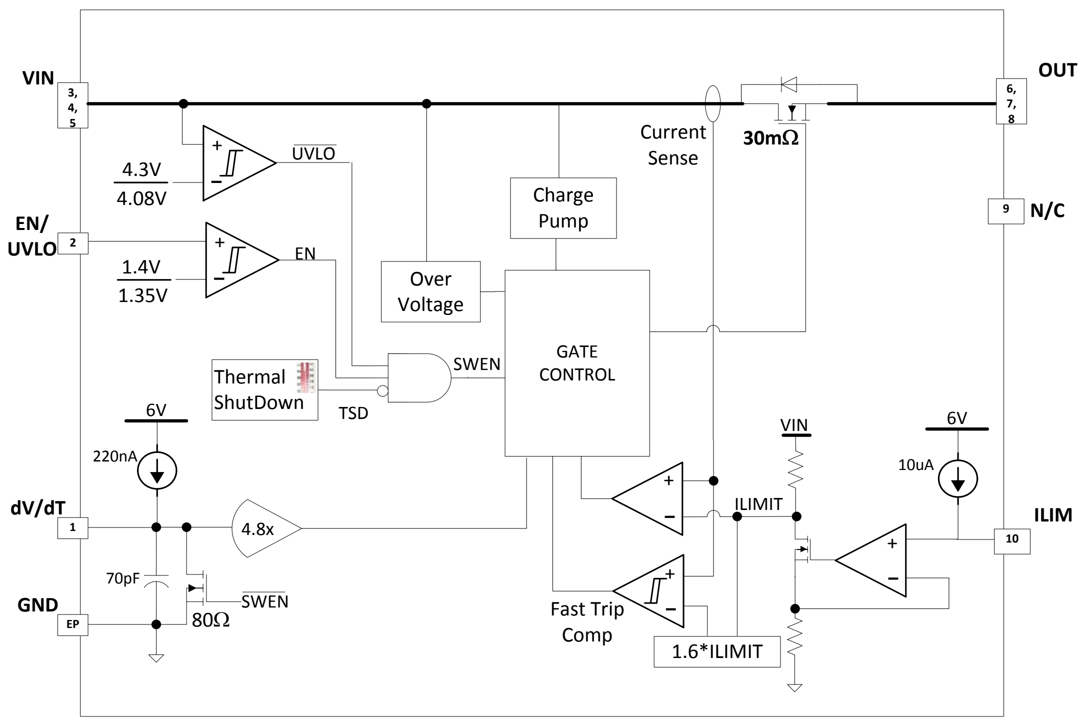
8 Detailed Description

8.1 Overview

The TPS25925x/6x is an e-fuse with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold (V_{UVR}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device will start conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (below V_{ENF}), internal MOSFET is turned off. User also has the ability to modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit IOL is not exceeded and input voltage spikes are safely clamped to VOVC level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature (T_J) exceeds TSHDN, typically 150°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. In TPS259250/60, the output will remain disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS259251/61 device will remain off and commences an auto-retry cycle of 145 ms after device temperature falls below T_{SHDN} – 10°C. This auto-retry cycle will continue until the fault is cleared.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 GND

This is the most negative voltage in the circuit and is used as a reference for all voltage measurements unless otherwise specified.

Feature Description (continued)

8.3.2 VIN

Input voltage to the TPS25925x/6x. A ceramic bypass capacitor close to the device from VIN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 4.5 V – 13.8 V for TPS25926x and 4.5 V – 5.5 V for TPS25925x. The device can continuously sustain a voltage of 20 V on VIN pin. However, above the recommended maximum bus voltage, the device is in over-voltage protection (OVP) mode, limiting the output voltage to V_{OVC}. The power dissipation in OVP mode is $P_{D\_OVP} = (V_{VIN} - V_{OVC}) \times I_{OUT}$, which can potentially heat up the device and cause thermal shutdown.

8.3.3 dV/dT

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum T_{dVdT}) on the output. Governing slew rate at start-up is shown in Equation 1.

$$\frac{dV_{OUT}}{dt} = \frac{I_{dVdT} \times GAIN_{dVdT}}{C_{dVdT} + C_{INT}} \quad (1)$$

Where:

I_{dVdT} = 220 nA (TYP)
C_{INT} = 70 pF (TYP)
$GAIN_{dVdT}$ = 4.85
$\frac{dV_{OUT}}{dT}$ = Desired output slew rate

The total ramp time (T_{dVdT}) for 0 to VIN can be calculated using the following equation:

$$T_{dVdT} = 10^{6} \times V_{IN} \times (C_{dVdT} + 70\ \text{pF}) \quad (2)$$

For details on how to select an appropriate charging time/rate, refer to the applications section *Setting Output Voltage Ramp Time (T_{dVdT})*.

8.3.4 EN/UVLO

As an input pin, it controls both the ON/OFF state of the internal MOSFET and that of the external blocking FET. In its high state, the internal MOSFET is enabled and charging begins for the gate of external FET. A low on this pin turns off the internal MOSFET and pull the gate of the external FET to GND via the built-in discharge resistor. High and Low levels are specified in the parametric table of the datasheet. The EN/UVLO pin is also used to clear a thermal shutdown latch in the TPS259250/60 by toggling this pin (H→L).

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (1 µs typical) for quick detection of power failure. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

8.3.5 ILIM

The device continuously monitors the load current and keeps it limited to the value programmed by R_{ILIM}. After start-up event and during normal operation, current limit is set to I_{OL} (over-load current limit).

$$I_{OL} = \left(0.7 + 3 \times 10^{-5} \times R_{ILIM}\right) \quad (3)$$

When power dissipation in the internal MOSFET [$P_D = (V_{VIN} - V_{OUT}) \times I_{OUT}$] exceeds 10 W, there is a 2% – 12% thermal foldback in the current limit value so that I_{OL} drops to I_{SC}. In each of the two modes, MOSFET gate voltage is regulated to throttle short-circuit and overload current flowing to the load. Eventually, the device shuts down due to over temperature.

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Feature Description (continued)

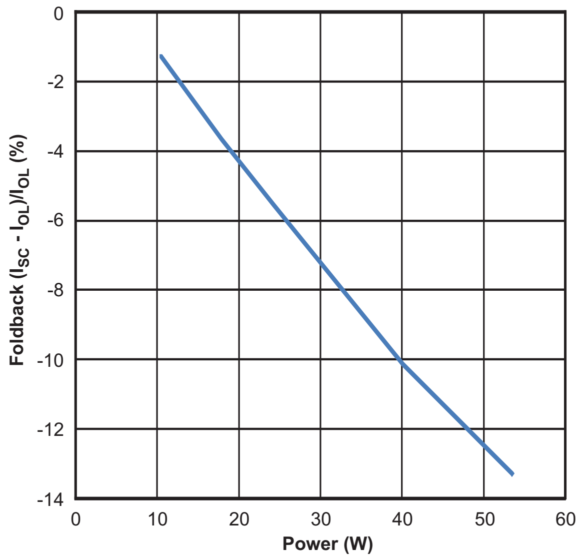

Figure 39. Thermal Foldback in Current Limit

During a transient short circuit event, the current through the device increases very rapidly. The current-limit amplifier cannot respond to this event due to its limited bandwidth. Therefore, the TPS25925/6 incorporates a fast-trip comparator, which shuts down the pass device when $I_{OUT} > I_{FASTRIP}$, and terminates the rapid short-circuit peak current. The trip threshold is set to 60% higher than the programmed over-load current limit ($I_{FASTRIP} = 1.6 \times I_{OL}$). After the transient short-circuit peak current has been terminated by the fast-trip comparator, the current limit amplifier smoothly regulates the output current to I_{OL} (see Figure 40).

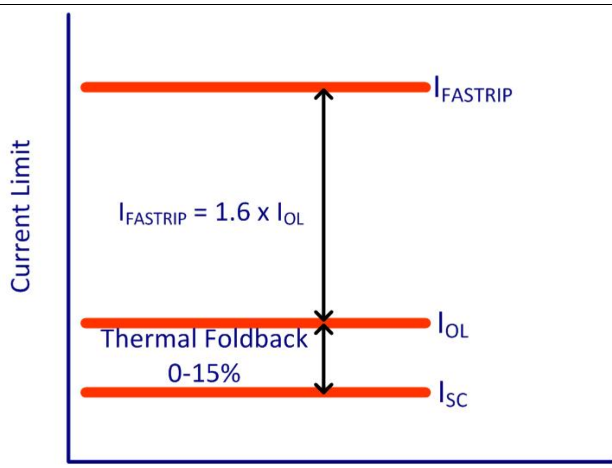

Figure 40. Fast-Trip Current

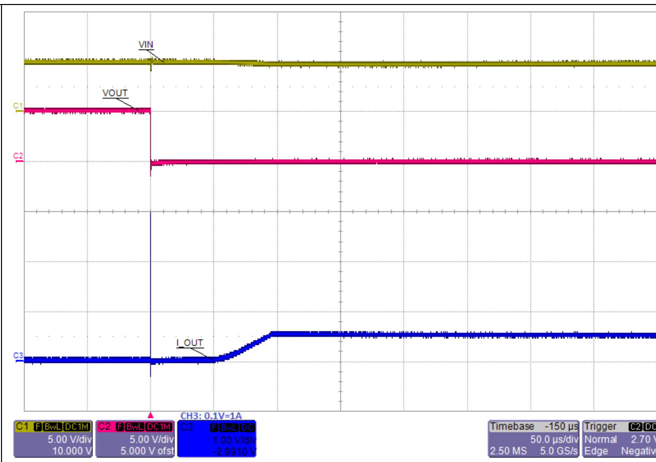

Figure 41. Fast-Trip and Current Limit Amplifier Response for Short Circuit

8.4 Device Functional Modes

The TPS25925x/6x is a hot-swap controller with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When V_{VIN} exceeds the undervoltage-lockout threshold (V_{UVR}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device and external FET (if connected) starts conducting and allows current to flow from VIN to OUT. When EN/UVLO is held low (that is, below V_{ENF}), the internal MOSFET is turned off; thereby, blocking the flow of current from VIN to OUT. The user can modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

Having successfully completed its start-up sequence, the device now actively monitors the load current and input voltage, ensuring that the adjustable overload current limit I_{OL} is not exceeded and input voltage spikes are safely clamped to V_{OVC} level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. If the device temperature (T_J) exceeds T_{SHDN}, typically 150°C, the thermal shutdown circuitry shuts down the internal MOSFET; thereby, disconnecting the load from the supply. In the TPS259250/60, the output remains disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS259251/61 device will remain off and commences an auto-retry cycle of 145 ms after device temperature falls below T_{SHDN} – 10°C. This auto-retry cycle will continue until the fault is cleared.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPA25925x/6x is a smart eFuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 4.5 V to 18 V with programmable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as Set-Top-Box, DTVs, Gaming Consoles, SSDs/HDDs and Smart Meters. The device also provides robust protection for multiple faults on the sub-system rail.

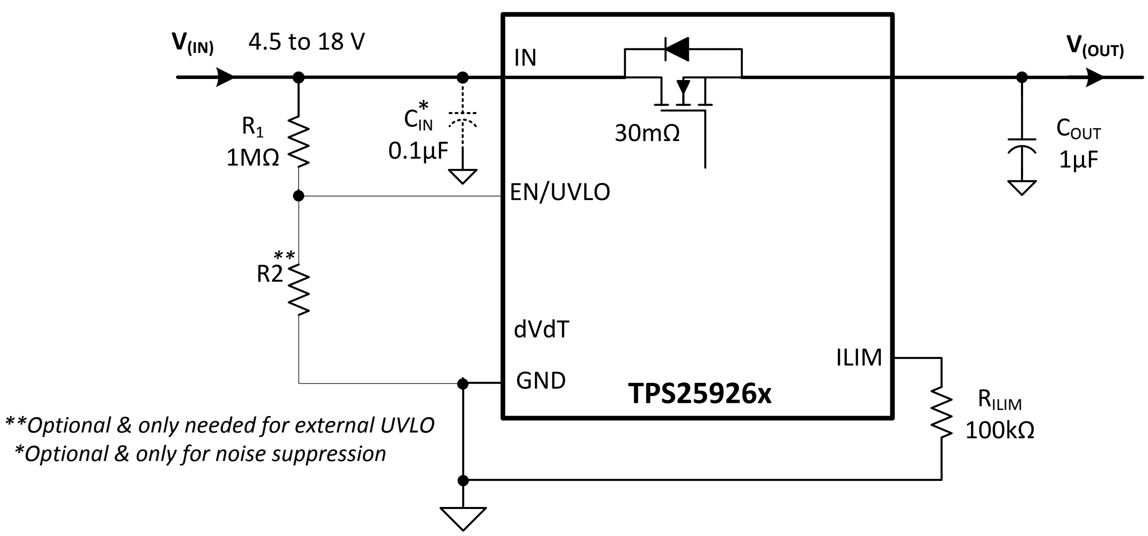
The following design procedure can be used to select component values for the device.

Alternatively, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool *TPS2592xx Design Calculator* (SLUC570) is available on web folder.

This section presents a simplified discussion of the design process.

9.2 Typical Application

9.2.1 Simple eFuse Protection for Set Top Boxes



* C_{IN} is optional and 0.1 µF is recommended to suppress transients due to the inductance of PCB routing or from input wiring.

Figure 42. Typical Application Schematic: Simple e-Fuse for STBs

9.2.1.1 Design Requirements

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range, V_{IN}	12 V
Undervoltage lockout set point, $V_{(UV)}$	Default: V_{UVR} = 4.3 V
Overvoltage protection set point , $V_{(OV)}$	Default: V_{OVC} = 15 V

Typical Application (continued)

Table 1. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Load at Start-Up, $R_{L(SU)}$	4 Ω
Current limit, I_{OL}	3.7 A
Load capacitance, C_{OUT}	1 µF
Maximum ambient temperatures, T_A	85°C

9.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS25926x.

9.2.1.2.1 Step by Step Design Procedure

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal input operation voltage
- Maximum output capacitance
- Maximum current Limit
- Load during start-up
- Maximum ambient temperature of operation

This design procedure below seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

9.2.1.2.2 Programming the Current-Limit Threshold: R_{ILIM} Selection

The R_{ILIM} resistor at the ILIM pin sets the over load current limit, this can be set using Equation 4.

$$R_{ILIM} = \frac{I_{ILIM} - 0.7}{3 \times 10^{-5}} \quad (4)$$

For ILIM = 3.7 A, from Equation 4, R_{ILIM} is 100 kΩ, choose closest standard value resistor with 1% tolerance.

9.2.1.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of R_1 and R_2 as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving Equation 5.

$$V_{(UV)} = \frac{R_1 + R_2}{R_2} \times V_{ENR} \quad (5)$$

Where V_{ENR} is enable voltage rising threshold (1.4 V). Since R1 and R2 will leak the current from input supply (Vin), these resistors should be selected based on the acceptable leakage current from input power supply (Vin).

The current drawn by R1 and R2 from the power supply $\{I_{(R12)} = V_{(IN)}/(R_1 + R_2)\}$.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I_{(R12)}$ must be chosen to be 20x greater than the leakage current expected.

For default UVLO of V_{UVR} = 4.3 V, select R2 = OPEN, and R_1 = 1 MΩ. Since EN/UVLO pin is rated only to 7 V, it cannot be connected directly to VIN = 12 V. It has to be connected through R_1 = 1 MΩ only, so that the pull-up current for EN/UVLO pin is limited to < 20 µA.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the rising threshold, V_{UVR}. This is calculated using Equation 6.

$$V_{(PFAIL)} = 0.96 \times V_{UVR} \quad (6)$$

Where V_{UVR} is 4.3 V, Power fail threshold set is : 4.1 V.

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9.2.1.2.4 Setting Output Voltage Ramp Time (T_{dVdT})

For a successful design, the junction temperature of device should be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor C_{dVdT} needed is calculated considering the two possible cases.

9.2.1.2.4.1 Case 1: Start-Up without Load: Only Output Capacitance C_{OUT} Draws Current During Start-Up

During start-up, as the output capacitor charges, the voltage difference as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using Equation 8.

For TPS25926x device, the inrush current is determined as,

$$I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{T_{dVdT}} \quad (7)$$

Power dissipation during start-up is:

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (8)$$

Equation 8 assumes that load does not draw any current until the output voltage has reached its final value.

9.2.1.2.4.2 Case 2: Start-Up with Load: Output Capacitance C_{OUT} and Load Draws Current During Start-Up

When load draws current during the turn-on sequence, there will be additional power dissipated. Considering a resistive load during start-up ($R_{L(SU)}$), load current ramps up proportionally with increase in output voltage during T_{dVdT} time. The average power dissipation in the internal FET during charging time due to resistive load is given by:

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V^2_{(IN)}}{R_{L(SU)}} \quad (9)$$

Total power dissipated in the device during startup is:

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (10)$$

Total current during startup is given by:

$$I_{(STARTUP)} = I_{(INRUSH)} + I_L(t) \quad (11)$$

If $I_{(STARTUP)} > I_{OL}$, the device limits the current to I_{OL} and the current limited charging time is determined by:

$$T_{dVdT(Current-Limited)} = C_{OUT} \times R_{L(SU)} \times \left[\frac{I_{OL}}{I_{(INRUSH)}} - 1 + LN\left(\frac{I_{(INRUSH)}}{I_{OL} - \frac{V_{(IN)}}{R_{L(SU)}}}\right)\right] \quad (12)$$

The power dissipation, with and without load, for selected start-up time should not exceed the shutdown limits as shown in Figure 43:

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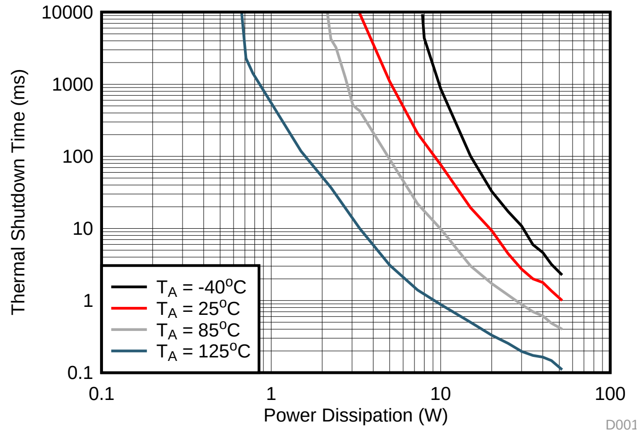

Figure 43. Thermal Shutdown Limit Plot

For the design example under discussion, select ramp-up capacitor C_{dVdT} = OPEN. Then, using Equation 2:

$$T_{dVdT} = 10^6 \times 12 \times (0 + 70\ pF) = 840\ \mu s \tag{13}$$

The inrush current drawn by the load capacitance (C_{OUT}) during ramp-up using Equation 14:

$$I_{(INRUSH)} = 1\ \mu F \times \frac{12}{840\ \mu s} = 15\ mA \tag{14}$$

The inrush power dissipation is calculated using Equation 15:

$$P_{D(INRUSH)} = 0.5 \times 12 \times 15\ m = 90\ mW \tag{15}$$

For 90 mW of power loss, the thermal shut down time of the device should not be less than the ramp-up time T_{dVdT} to avoid the false trip at maximum operating temperature. From thermal shutdown limit graph Figure 43 at T_A = 85°C, for 90 mW of power, the shutdown time is infinite. So it is safe to use 0.79 ms as start-up time without any load on output.

Considering the start-up with load 4 Ω, the additional power dissipation, when load is present during start up is calculated using Equation 9:

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 4} = 6\ W \tag{16}$$

The total device power dissipation during start up is:

$$P_{D(STARTUP)} = 6 + 90\ m = 6.09\ W \tag{17}$$

From thermal shutdown limit graph at T_A = 85°C, the thermal shutdown time for 6.09 W is more than 10 ms. So it is well within acceptable limits to use no external capacitor ($C_{dV/dT}$) with start-up load of 4 Ω.

If, due to large C_{OUT}, there is a need to decrease the power loss during start-up, it can be done with increase of C_{dVdT} capacitor.

9.2.1.2.5 Support Component Selection - C_{VIN}

C_{VIN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended for C_{VIN}.

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9.2.1.3 Application Curves

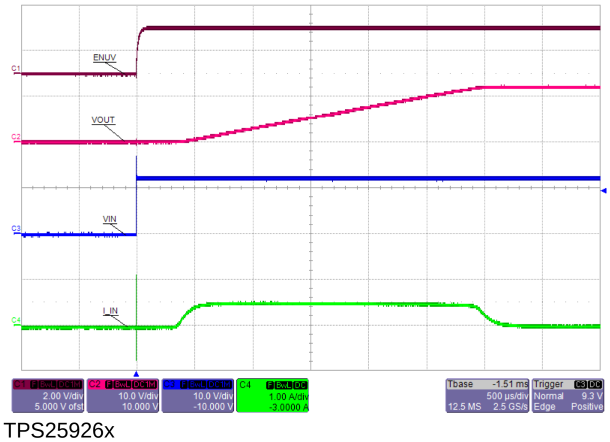


Figure 44. Hot-Plug Start-Up: Output Ramp without Load on Output

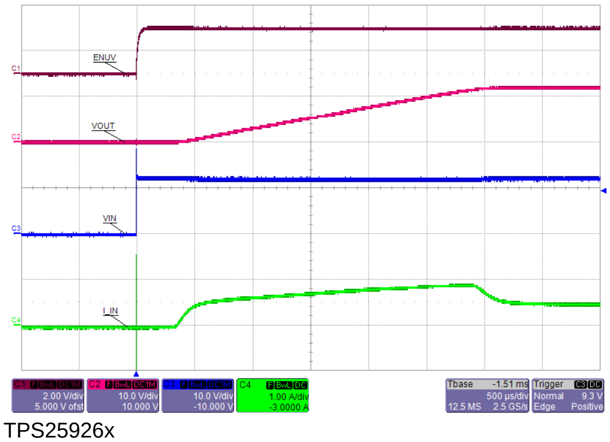


Figure 45. Hot-Plug Start-Up: Output Ramp with 24-Ω Load at Start Up

10 Power Supply Recommendations

The device is designed for supply voltage range of 4.5 V ≤ V_{IN} ≤ 18 V. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply should be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

10.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

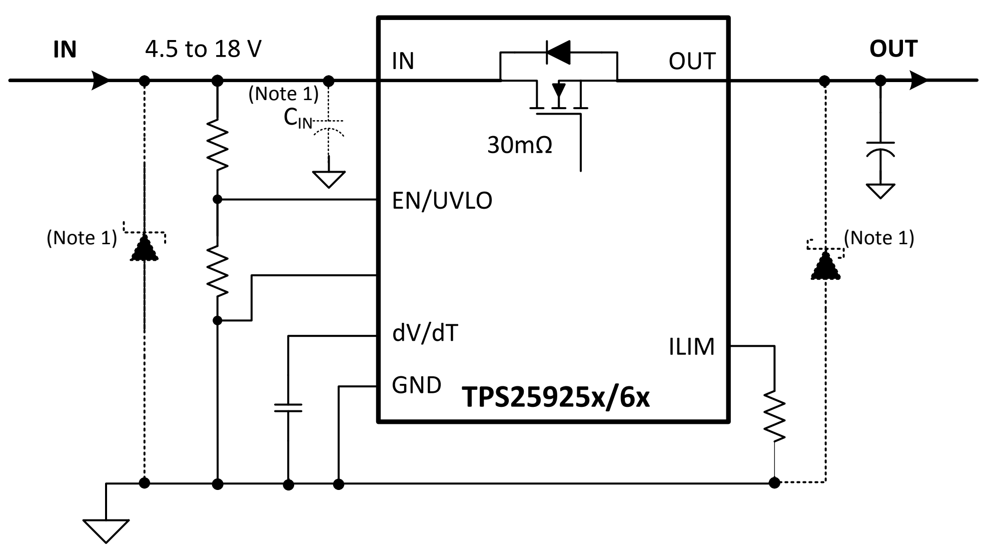
Typical methods for addressing transients include:
- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ = 0.001 µF to 0.1 µF) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with Equation 18:

$$V_{SPIKE(Absolute)} = V_{(IN)} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (18)$$

Where:
- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 46.



(1) Optional components needed for suppression of transients

Figure 46. Circuit Implementation with Optional Protection Components

PRODUCT PREVIEW

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

11 Layout

11.1 Layout Guidelines

- For all applications, a 0.01-µF or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated/minimized.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure 47 for a PCB layout example.
- High current carrying power path connections should be as short as possible and should be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground should be a copper plane or island on the board.
- Locate all TPS25925x/6x support components: R_{ILIM}, C_{dVdT} and resistors for ENUV, close to their connection pin. Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILIM} and C_{dVdT} components to the device should be as short as possible to reduce parasitic effects on the current limit and soft start timing. These traces should not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it should be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible; however this layout has been shown to produce good results and is intended as a guideline.

11.2 Layout Example

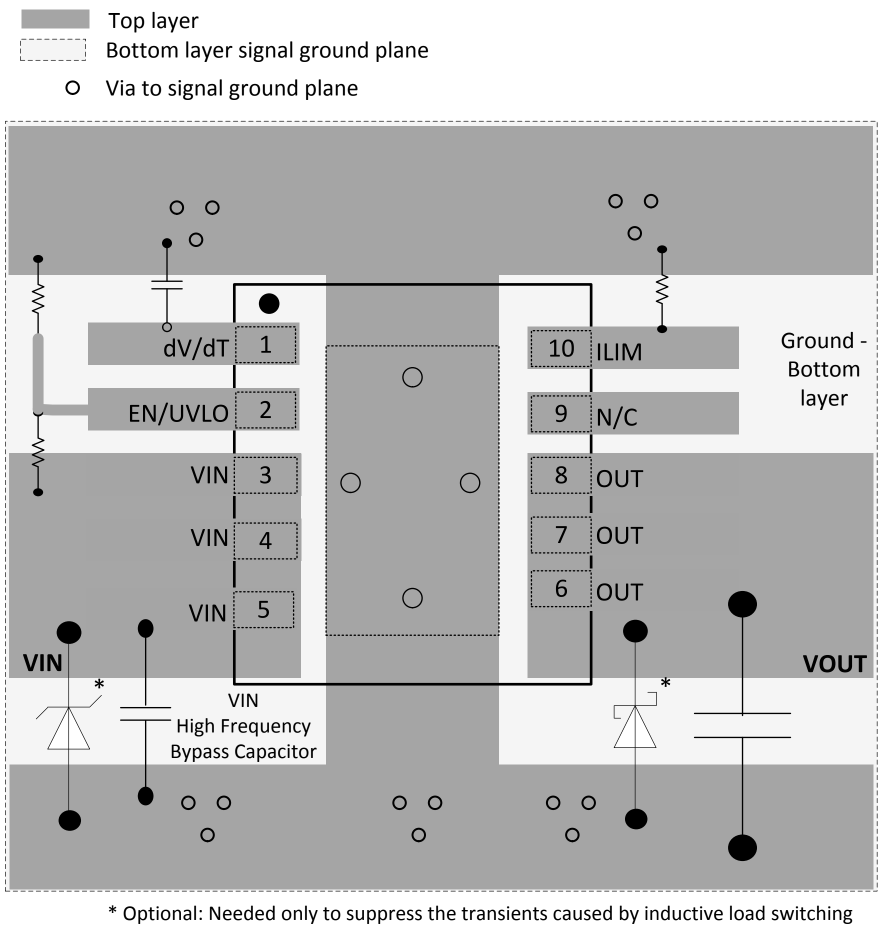


Figure 47. Layout Example

PRODUCT PREVIEW

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

TPS2592xx Design Calculator (SLUC570)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS259250	Click here	Click here	Click here	Click here	Click here
TPS259251	Click here	Click here	Click here	Click here	Click here
TPS259260	Click here	Click here	Click here	Click here	Click here
TPS259261	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

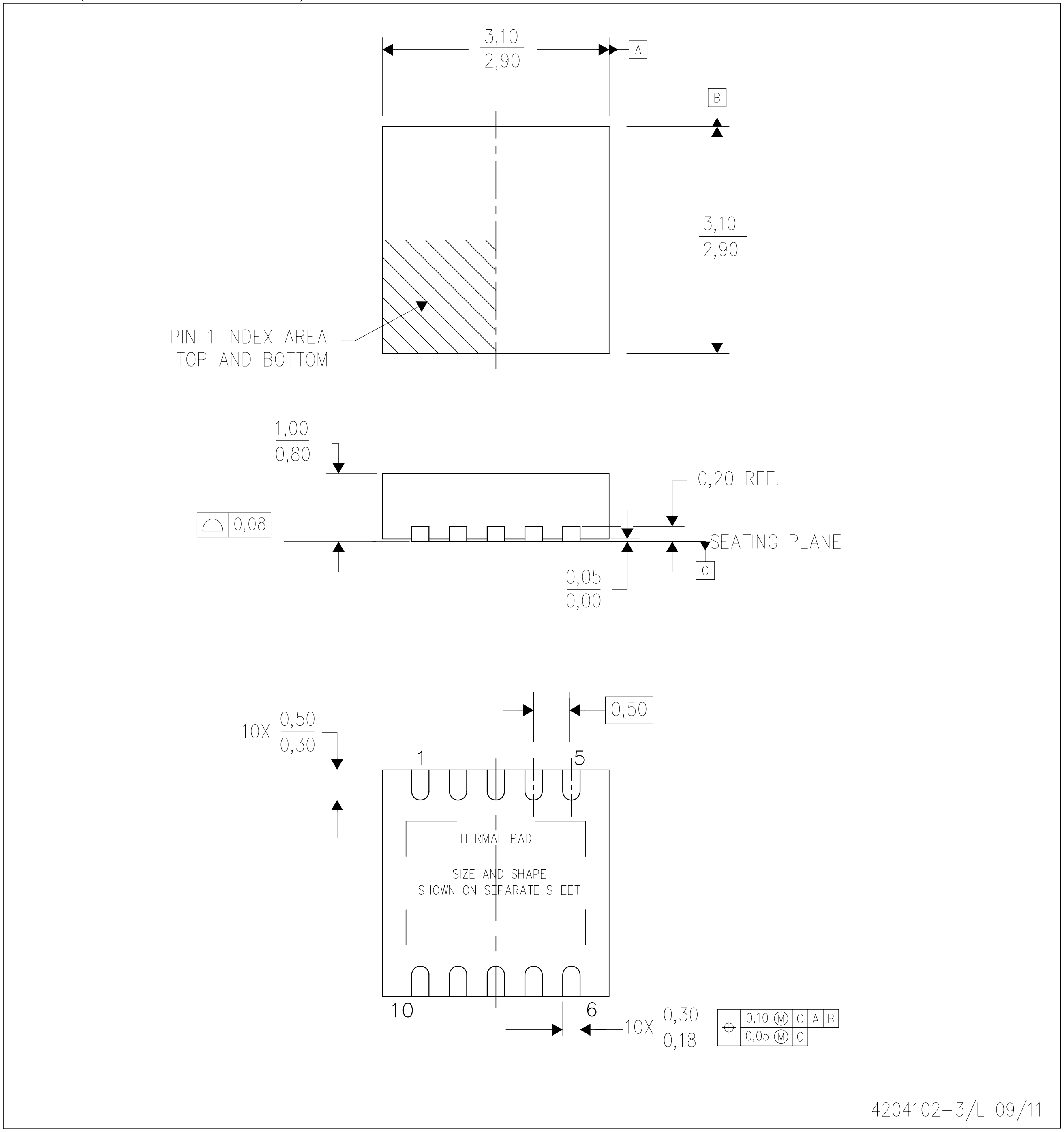
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

Products		**Applications**	
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